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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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10/727,198

12/02/2003

Simon Robert Walmsley

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SILVERBROOK RESEARCH PTY LTD  
393 DARLING STREET  
BALMAIN, 2041  
AUSTRALIA

EXAMINER
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LE, DINH THANH

ART UNIT	PAPER NUMBER
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2816

MAIL DATE	DELIVERY MODE
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09/05/2007

PAPER

**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

**Office Action Summary**

Application No.

10/727,198

Applicant(s)

WALMSLEY, SIMON ROBERT

Examiner

DINH T. LE

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 03 July 2007.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 1 and 3-6 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1 and 3-6 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a) (d) or (f).
- a) ☐ All b) ☐ Some \* c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
  2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- |  |   |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)                                | 4) <input type="checkbox"/> Interview Summary (PTO-413)<br>Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)                       | 5) <input type="checkbox"/> Notice of Informal Patent Application                       |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08)<br>Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____  |

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***FINAL REJECTION***

***Claims Rejections***

***Claim Rejections - 35 USC § 112***

Claims 1 and 3-6 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Correction or clarification is required.

In claim 1, it is not understood how the filter can “alter” the system clock when it is not connected to anything and how the clock filter can be “configured” to detect an under temperature condition” since the filter is the means for filtering unwanted noise, and how the recitation “filter configured to detect an under temperature condition” is read on the preferred embodiment or seen on the drawings. The recitation “an under temperature condition” on line 5 is confusing because it is unclear if this is additional “condition” or further recitation of the previously claimed “condition” on line 3.

The remaining claimed are dependent from claim 1 and therefore also considered indefinite.

***Claim Rejections - 35 USC § 102***

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this

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subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claim 1 is rejected under 35 USC 102 (e) as being anticipated by Uchida et al (US 6,731,919).

As the best construed, Uchida et al discloses in Figure 1 a circuit comprising:

a clock filter (4, 18) configured to determine a detect an under temperature condition of the integrated circuit, at which the temperature is below a predetermined temperature, and to alter an output of the system clock (8) in the event that under temperature condition is below a predetermined temperature, see 1-11, column 10.

Claim 1 is rejected under 35 USC 102 (e) as being anticipated by Yamazaki (JP409212254)

As the best construed, Yamazaki discloses in Figure 1 a circuit comprising:

a clock filter (1-3 ) configured to determine a detect an under temperature condition of the integrated circuit (8), at which the temperature is below a predetermined temperature, and to alter an output of the system clock (7) in the event that under temperature condition is below a predetermined temperature.

### ***Claim Rejections - 35 USC § 103***

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 1 and 3-6 are rejected under 35 U.S.C. 103 (a) as being unpatentable over Chemla (U.S Patent No. 5,805,403) in view of Yamazaki (JP409212254)..

Chemla discloses in figs. 1-5 an integrated circuit temperature monitoring and protection system including: an on-board system clock (CLOCK), the integrated circuit (10) including a clock filter (20) configured to determine a temperature of the integrated circuit (60 determine a temperature for the integrated circuit 10) and to alter an output of the system clock (CLOCK).

Regarding claim 3, altering the output includes preventing the clock signal from reaching one or more logical circuits on the integrated circuit to which it would otherwise be applied (when switch 46 is open).

Regarding claim 4, the predetermined temperature range is selected such that a temperature-related speed of the system clock output that is not due to the clock filter is within a predetermined frequency range (inherently seen in the abstract and the summary of the Chemla's reference).

Regarding claim 5, the frequency range is within an operating frequency of some or all of the logic circuitry to which the system clock is supplied (inherently seen in the abstract and the summary of the Chemla's reference).

Regarding claim 6, the temperature range is bounded at a lower level such that an output of the system clock is prevented from reaching some or all of the logic circuitry prior to race conditions due to low temperature causing unpredictable logical behavior (see cols. 3-6).

However, Chmla does not disclose that the detected temperature is below a predetermined temperature.

Nevertheless, Yamazaki suggests in Figure 1 a detection circuit (3, 2, 1) for detecting a temperature of the chip (8) below a predetermined temperature to improve reliability by stabilizing clock margin, see the Abstract.

It would have been obvious to a person having skill in the art at the time the invention was made to incorporate the suggestion of Yamazaki into the circuit of Chemla for the purpose of detecting the temperature below a predetermined temperature to stabilize the clock margin.

Claims 1 and 3-6 are, insofar as understood, rejected under 35 U.S.C. 103(a) as being unpatentable over Kitano (U.S Patent No. 5,870,267) in view of Yamazaki (JP409212254).

Kitano discloses in Figs. 1-2 a semiconductor integrated circuit device including: the integrated circuit (Fig. 1) including an on-board system clock (CK, Fig. 2), the integrated circuit (Fig. 1) including a clock filter (4) configured to determine a temperature of the integrated circuit (Fig. 1) and to alter an output of the system clock (CK) based on the temperature as recited in claim 1. See the abstract, lines 6 - last line.

Regarding claims 3-6, figs. 1-2 of Kitano is capable of performing the function as recited in these claims. See col. 5, lines 8-21.

However, Kitano does not disclose that the detected temperature is below a predetermined temperature.

Nevertheless, Yamazaki suggests in Figure 1 a detection circuit (3, 2, 1) for detecting a temperature of the chip (8) below a predetermined temperature to improve reliability by stabilizing clock margin, see the Abstract.

It would have been obvious to a person having skill in the art at the time the invention was made to incorporate the suggestion of Yamazaki into the circuit of Kitano for the purpose of detecting the temperature below a predetermined temperature to stabilize the clock margin.

***Response to Applicant's Arguments***

The applicant argues that Chemla merely discloses either halting a clock signal within an integrated circuit, or resetting the integrated circuit when a temperature above a threshold temperature is detected (see col. 3, line 48-col. 4, line 44 of Chemla). Kitano merely discloses either operating cooling fans and/or reducing processing of data in an integrated circuit when a temperature above a first threshold temperature is detected, or stopping a clock signal within the integrated circuit when a temperature above a higher, second threshold temperature is detected (see col. 5, line 8-52 of Kitano). The arguments are moot. However, detection of the temperature below a predetermined temperature is suggested by Yamazaki as stated above.

***Conclusion***

1. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire **THREE MONTHS** from the mailing date of this action. In the event a first reply is filed within **TWO MONTHS** of the mailing date of this final action and the advisory action is not mailed until after the end of the **THREE-MONTH** shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than **SIX MONTHS** from the mailing date of this final action.

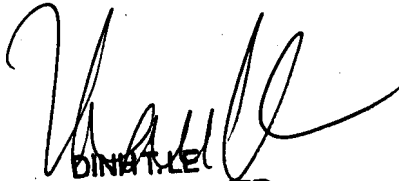
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Any inquiry concerning this communication or earlier communications from the examiner should be directed to DINH T. LE whose telephone number is (571) 272-1745. The examiner can normally be reached on Monday-Friday (8AM-7PM).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Drew Richards, can be reached at (571) 272-1736.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

8/22/07

  
DINH T. LE  
PRIMARY EXAMINER